WE CLAIM:

1. In a multiprocessor digital signal processing system, the combination comprising a single coder/decoder having a digital/analog conversion channel time division multiplexed among, and an analog/digital conversion channel concurrently coupled to, the multiple processors thereof.

2. The combination of Claim 1 including means individually selecting input digital signals and analog signals for digital/analog conversion and analog/digital conversion, respectively, and assigning which of the multiple processors in the system couples output to the digital/analog conversion channel.

3. A digital signal processing system comprising:

a single coder/decoder having digital and analog signal inputs, and digital/analog and analog/digital conversion channels;

a first source of analog input signals coupled to said analog signal input of said coder/decoder;

a second source of digital input signals;

a first plurality of signal processors coupled between said source of digital input signals and said digital signal input of said coder/decoder; and

means time division multiplexing said digital/analog

conversion channel of said coder/decoder;

whereby digital-to-analog converted signals are time division multiplexed at said analog output of said coder/decoder, and analog-to-digital converted signals are concurrently accessible at such digital output of said coder/decoder.

4. The digital signal processing system of Claim 3 also including a second plurality of signal processors coupled to said digital output of said coder/decoder for operating on said analog-to-digital converted signals.

5. The digital signal processing system of Claim 4 wherein said first plurality of signal processors also include a plurality of registers to buffer digital signal data for use by said coder/decoder.

6 The digital signal processing system of Claim 5 wherein said second plurality of signal processors also include a plurality of registers to buffer digital signal data from said coder/decoder.

7. The digital signal processing system of Claim 6 wherein said means includes a multiprocessor for individually selecting digital signals and analog signals from said first and second sources for digital-to-analog and analog-to-digital conversions, respectively, by said coder/decoder.